APPENDIX

MD800G6

Grayscale 800 × 600 MicroMonitor

I. General Description

The MD800G6 device is an active matrix liquid crystal display with 800 × 600 spatial resolution. Integrated horizontal and vertical shift registers reduce driving logic. The device is easy to interface, with a single (monochrome) or four (color) analog video inputs and six digital inputs.

Line timing supports interlaced and non-interlaced scanning, as well as windowing of a larger virtual display. Rows and columns are driven sequentially in raster order. The display supports externally generated, and therefore arbitrary, inversion patterns, including frame, row, column, and pixel inversion.

Features

- 800 (H) by 600 (V) spatial resolution
- 5 V analog video input
- Low power consumption: 30 mW worst case for 60 Hz monochrome and 25 mW for color
- Integrated horizontal and vertical shift registers
- Interlaced and non-interlaced capabilities
- 12.55 µm pixel pitch

Applications

- Cellular/PCS Phones
- Pocket Pagers
- Portable Projectors
- Watches
- Personal Digital Assistants
- GPS Viewers
- Camcorder Viewfinders
- Low-Cost Projectors
- Flat Desktop Monitors
- Virtual Reality Goggles
- Video Games

Display Package

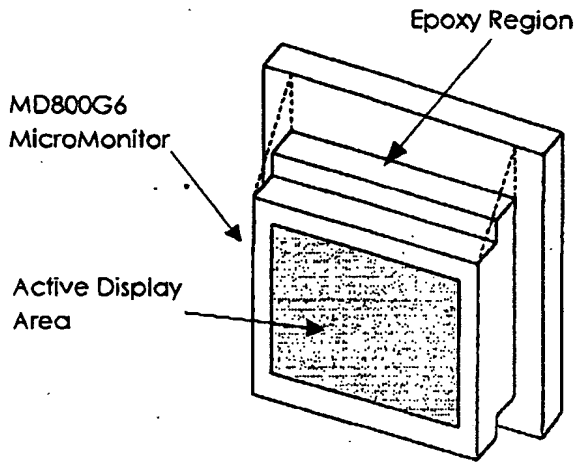

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TABLE 1: Preliminary Specifications

General

Display Type	Grayscale Active Matrix Liquid Crystal Display on CMOS Backplane.
Number of Pixels	800 × 600 (480,000)
Pixel Pitch	12.55 µm
Pixel Fill Factor	89%
Grayscale	Continuous with up to 8 bits.
Driving Scheme	Optional field, column, or row inversion.

Electronic

Power Consumption	25 mW @ 180 Hz (worst case).
Interface	Digital Control, Analog Video.
Display logic Voltage	5 V
Frame Rate	60 -270 Hz
Pixel Update Rate	20 ns for 8 bit monochrome. 4 pixels per 20 ns clock for 8 bit color.

Liquid Crystal Material

Display Mode	Reflective, Normally White, Nematic LC Material.
Contrast Ratio	
Direct View in ambient illumination	>50:1
With f/2 viewing optics	>100:1
LC Viewing Angle	160°
Switching Speed (10% - 90%)	1.2 ms Bright to Dark, 5 ms Dark to Bright.
Video Voltage Range	0 - 5.0 V

Mechanical

Pixel Array	10.04 mm x 7.53 mm
Pixel Array + Display Frame	10.17 mm x 7.66 mm
Dimensions of Display Cell	12.13 mm x 10.80 mm
Weight of Display	.3 g

Environmental

Operating Temperature	0° C - 45° C
Storage Temperature	-20° C - 75° C

Figure 1: Functional Block Diagram

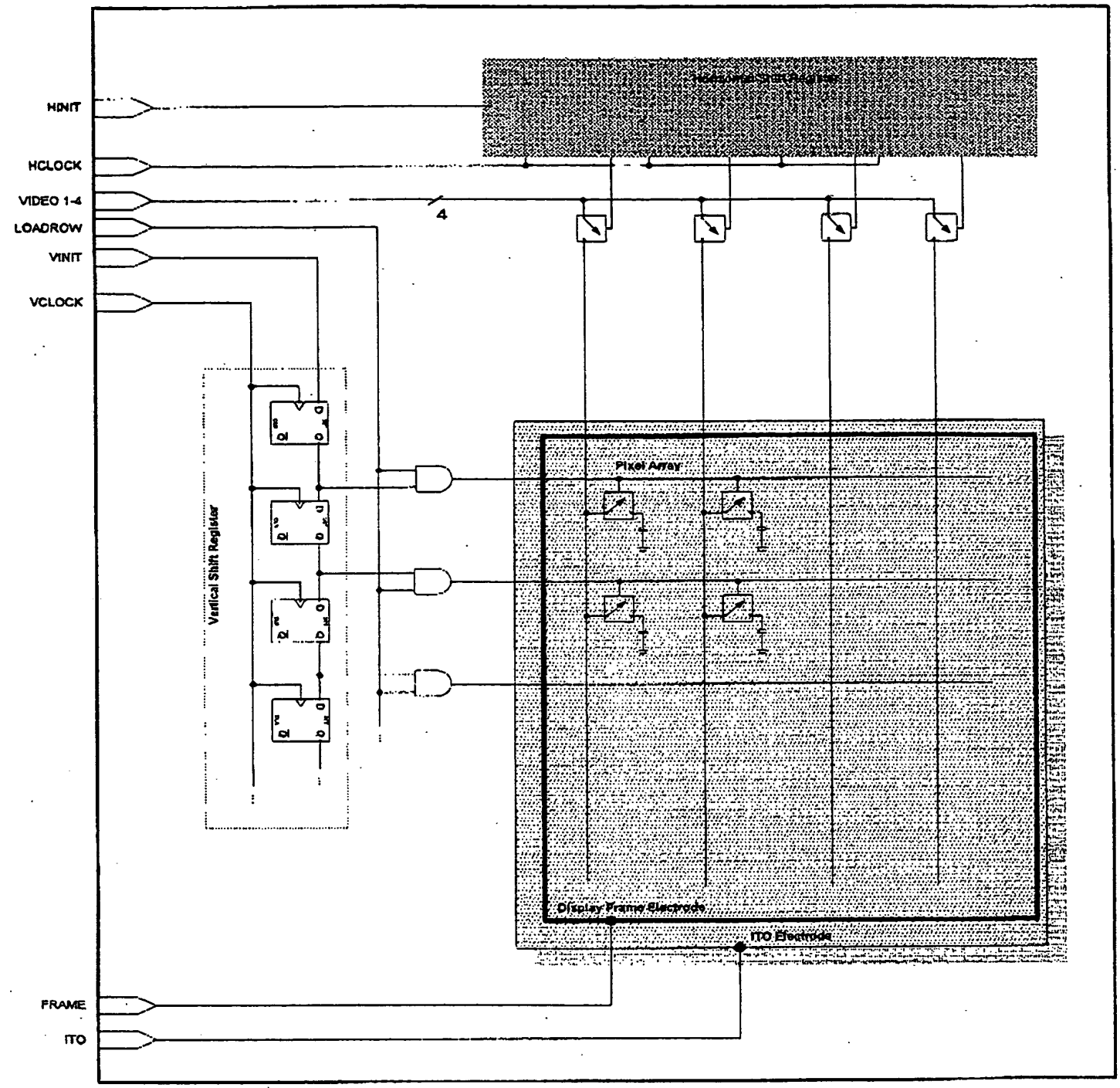


TABLE 2: Display Signals

Name	Description
VIDEO1	Analog video input - drives columns 1, 5, 9,...
VIDEO2	Analog video input - drives columns 2, 6, 10,....
VIDEO3	Analog video input - drives columns 3, 7, 11,....
VIDEO4	Analog video input - drives columns 4, 8, 12,...
VINIT	Initialization signal - vertical shift register.
VCLOCK	Vertical shift register clock.
HINIT	Initialization signal - horizontal shift register.
HCLOCK	Horizontal shift register clock.
FLASHCLEAR	Connects entire pixel array to FLASHVAL.
FLASHVAL	Flash-clear analog input - drives entire pixel array when FLASHCLEAR is asserted.
FRAME	Display frame voltage.
SBSEL	Single-bank select - operates display in single-bank mode when set high and multi-bank mode when set low.
ITO	Connection to transparent electrode on coverglass.
LOADROW	Loads video data into addressed pixel row (tie high).
GROUND	Ground.

TABLE 3: Absolute Maximum Ratings

Parameter/Condition	Symbol	Rated Value	Units
Supply Voltage	V_{DD}	4.5 to 5.5	V
Video Signal	V_{VID}	-0.5 to V_{DD}	V
Timing Inputs	V_{IN}	-0.5 to V_{DD}	V
Temperature - Operating	T_{OP}	0 to 45	°C
Temperature - Storage	T_{STOR}	-20 to 75	°C

Note: Stresses greater than those listed in the above table may cause permanent damage to the device.

ESD Warning

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. However, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either supply voltage or ground, unless otherwise noted elsewhere in this data sheet.

2. DC Operating Conditions and Characteristics

TABLE 4: Electrical Characteristics and Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	4.5	5	5.5	V
Operating Current: Power Supply: Source	I_{VDD}			5	mA
Video Signal Center Voltage	V_{SCV}		$V_{DD}/2$		V
Video Signal Range	$V_{VIDRANGE}$	0		V_{DD}	V
ITO Voltage	V_{ITO}	V_{scv}-0.5	V_{scv}	V_{scv}+0.5	V
Input High (Logic 1) Voltage	V_{IH}	3.3		5.5	V
Input Low (Logic 0) Voltage	V_{IL}	0		1	V
Input Current (except video, FLASHCLEAR)	V_{IN}			10	uA
FLASHVAL high voltage	V_{FVH}		3.5		V
FLASHVAL low voltage	V_{FVL}		1.5		V

TABLE 5: Display Power Consumption

Parameter	Symbol	Min.	Typ.	Max.	Units
60 frames per second operation (mono)	PWR_{M60}			30	mW
72 frames per second operation (mono)	PWR_{M72}			34	mW
60 frames/180 fields per second operations (FSC)	PWR_{F180}			25	mW

Table 5 only provides the consumption of the display cell, not including the illuminator. In typical portable display applications, an LED illuminator will draw 60 mA @ 5 V with a duty cycle of 24%, resulting in 72 mW average illuminator power consumption.

TABLE 6: Capacitance

Parameter	Symbol	Min.	Typ.	Max.	Units
Input Capacitance: HINIT, HCLOCK, LOADROW, VINIT, VCLOCK	C_C			12	pF
Input Capacitance: VIDEO	C_V			34	pF
Input Capacitance: FRAME	C_{BB}			84	pF

3. AC Operating Conditions and Characteristics

TABLE 7: Electrical Characteristics and Recommended AC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
HINIT setup	HS	5			ns
HINIT hold	HH	10			ns
HCLOCK high time	HCHI	7	12.5	100,000	ns
HCLOCK low time	HCLO	7	12.5	100,000	ns
VCLOCK, HINIT high time	VCHI	30	75		ns
VINIT setup	VS	5			ns
VINIT hold	VH	10			ns
LC Bright to Dark 90% - 10%	tS		1.2		ms
LC Dark to Bright 10% - 90%	tR		5		ms
FLASHVAL setup	FVS		0		ns
FLASHVAL high time	FCHI		2		ms
FLASHVAL HOLD	FVH		10		ns
FLASHCLEAR low before line start	FCLD	0			ns
Video valid before HCLOCK rising edge	VVCH	15			ns
Video hold time	VHCH	5			ns

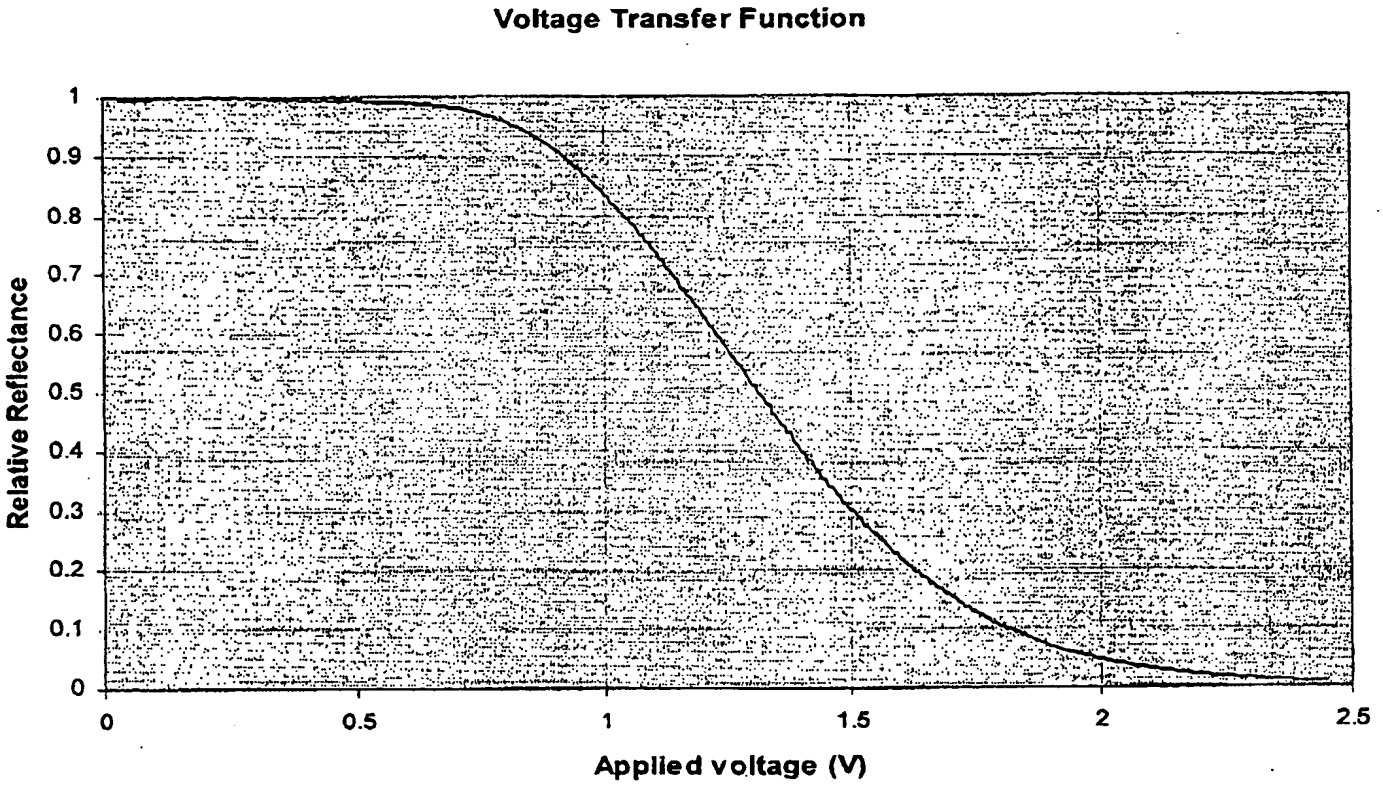
Note: AC characteristics assume signal transition times of 3 ns. Input transition times are measured from VIH (min) to VIL (max), and from VIL (max) to VIH (min). All control signals must transition in a monotonic manner.

4. Optical Characteristics

The liquid crystal mode used in MD800G6 optimizes the display contrast for an applied voltage of 2.4 V or less between ITO and the pixel electrodes. It uses a "normally bright" state that is bright when no voltage is applied, and darkens as the voltage increases.

The relationship between the voltage applied to the liquid crystal and the apparent brightness is called the Voltage Transfer Function (VTF). The characteristics of the liquid crystal make this a nonlinear function, as shown in Figure 2. Note that the display remains bright for voltages up to about 0.5 V. The brightness then starts dropping rapidly and asymptotically approaches the ultimate dark state. One useful approximation to this curve is a straight line.

Figure 2: MD800G6 VTF

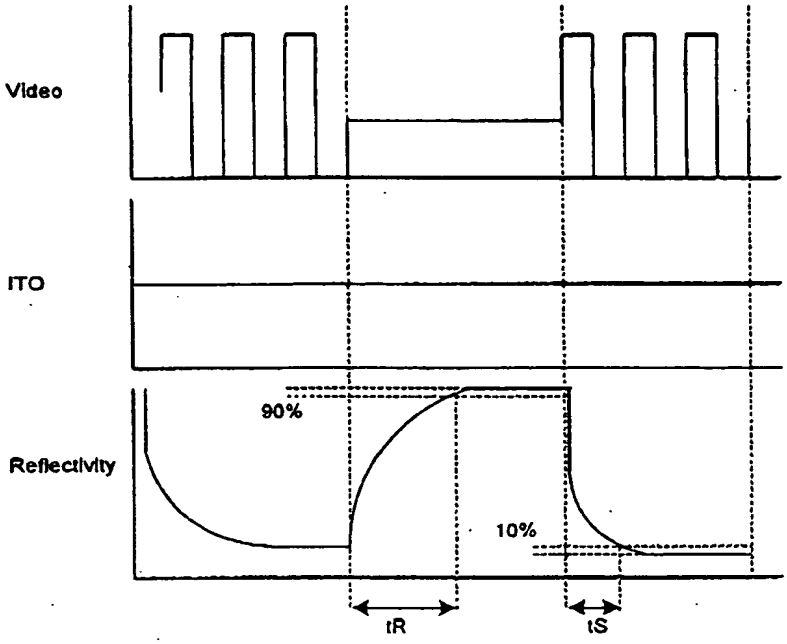


The VTF is measured by applying a square wave at 30 Hz to the video input and applying the appropriate timing signals to write the signal to each pixel in the display in each half-cycle. This mimics the waveform seen by the pixels when displaying a 60 Hz VGA source and toggling the polarity of the applied voltage each frame.

The brightness is measured with an incandescent light source and either a photopically filtered detector or a spectrophotometer to give the proper weighting to the response at each wavelength of light. The voltage amplitude of the square wave and the corresponding brightness produce one point on the VTF. Varying the voltage amplitude from 0 to 2.4 V produces the entire function. The ratio of brightnesses between 0 and 2.4 V applied to the display is the stated contrast ratio of the display.

The display turns on (darkens) more quickly than it relaxes (brightens). As Figure 3 shows schematically, the switching time tS and relaxation time tR are defined by the 10% and 90% transition levels, respectively.

Figure 3: MD800G6 tS and tR



5. Theory of Operation

Analog System

There are three key points regarding driving the LC material.

1. The voltage applied to the liquid crystal at any pixel is determined by the difference in voltage between that pixel's electrode and the ITO electrode on the other side of the LC material. The LC material responds to the RMS applied voltage, so that the voltage applied between the pixel and the cover glass electrode may change polarity without affecting the display.
2. The display MUST be driven with an AC voltage of zero DC bias to avoid impurity concentrations on the electrodes. Thus if a voltage P is desired across the liquid crystal, the pixel voltage must toggle between $V_{ITO} + P$ and $V_{ITO} - P$, where V_{ITO} is the voltage on the ITO electrode. ***Warning: a two-V DC voltage applied to the display for ten seconds visibly alters the display performance.***
3. The VTF is non-linear, so that intensity values must be transformed into voltage levels by a curve-fitting approach. Thus, image values must be mapped to the two 1.8 V ranges between 0 V and 1.8 V, and between 3.2 V and $V_{dd} = 5$ V.

Using the straight line approximation to the VTF:

$$V_{pixel} \begin{cases} V_{scv} + 0.7\ V + 1.8 * G & \text{even field} \\ V_{scv} - 0.7\ V - 1.8 * G & \text{odd field} \end{cases}$$

where G ranges between zero (white) and one (black).

The most common driving scheme sets the V_{ITO} permanently at the voltage midpoint of the chip (2.5 V) and alternates between writing fields of data first above and then below ITO. The ideal driver would exactly balance the applied voltages by writing exactly the same data to the display twice, once with each polarity. However, when working with continuous data streams, it suffices to alternate the polarity of successive frames, even though each frame's data will be slightly different.

Figure 4: Video Signal Polarity

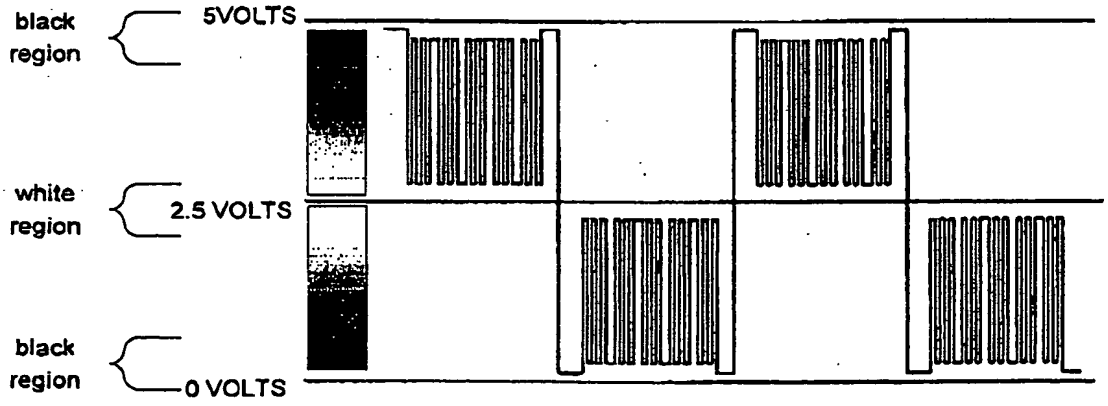


Figure 4 shows a typical video signal applied to the display. Every other video frame is inverted about the 2.5 VITO level. Notice that the voltage corresponding to the whitest intensity does not actually reach ITO.

Digital System

From an electronic point of view, the pixel array of an MD800G6 display consists of dynamic charge-storage nodes whose voltage determines the pixel brightness. Access to a particular pixel is controlled by horizontal and vertical shift registers, as shown in Figure 4. The vertical shift register (VSR) selects one of the 600 rows of pixels, while the horizontal shift register (HSR) controls the 800 column lines. The HSR outputs control which of the columns are connected to the video inputs. As the HSR is advanced, each selected column samples the video data via a track-and-hold mechanism. The selected column lines track the voltage on their video inputs at the start of the pixel interval and maintain the voltage after the switches are turned off.

Throughout the column loading sequence, the pixels of the current row in the pixel array (as selected by the VSR) are connected to the column lines.

The MD800G6 supports two variants of the basic mode described above. *Single-bank* mode is designed for lower-speed grayscale operation, while *multi-bank* mode is designed for high-speed field-sequential color operation. In single-bank mode, all four video lines are connected together on the display carrier, creating a single-input device, and each HCLOCK pulse advances the shift register by a pixel. In the multi-bank mode, the four video lines remain separate, allowing four pixel values to be loaded in a single HCLOCK cycle. Each HCLOCK pulse advances the shift register by four pixels. The following sections provide detailed descriptions of each mode.

Note: The LOADROW signal should be tied high when implementing the driving schemes described in this document. LOADROW should be controlled by the user only when implementing more advanced functions such as video deinterlacing. Please inquire with MicroDisplay for more information on this topic.

Figure 5: Functional diagram, single-bank mode

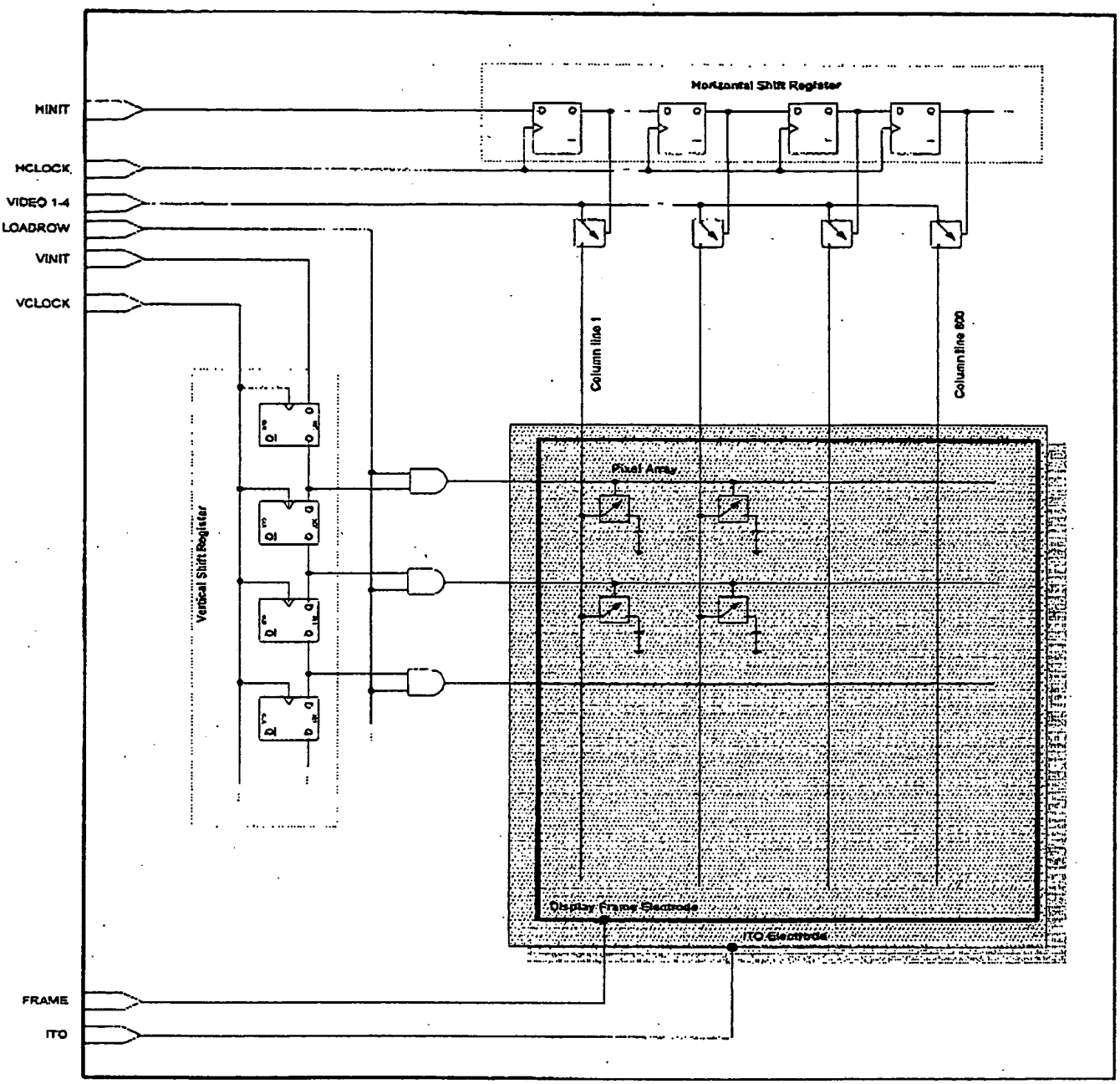
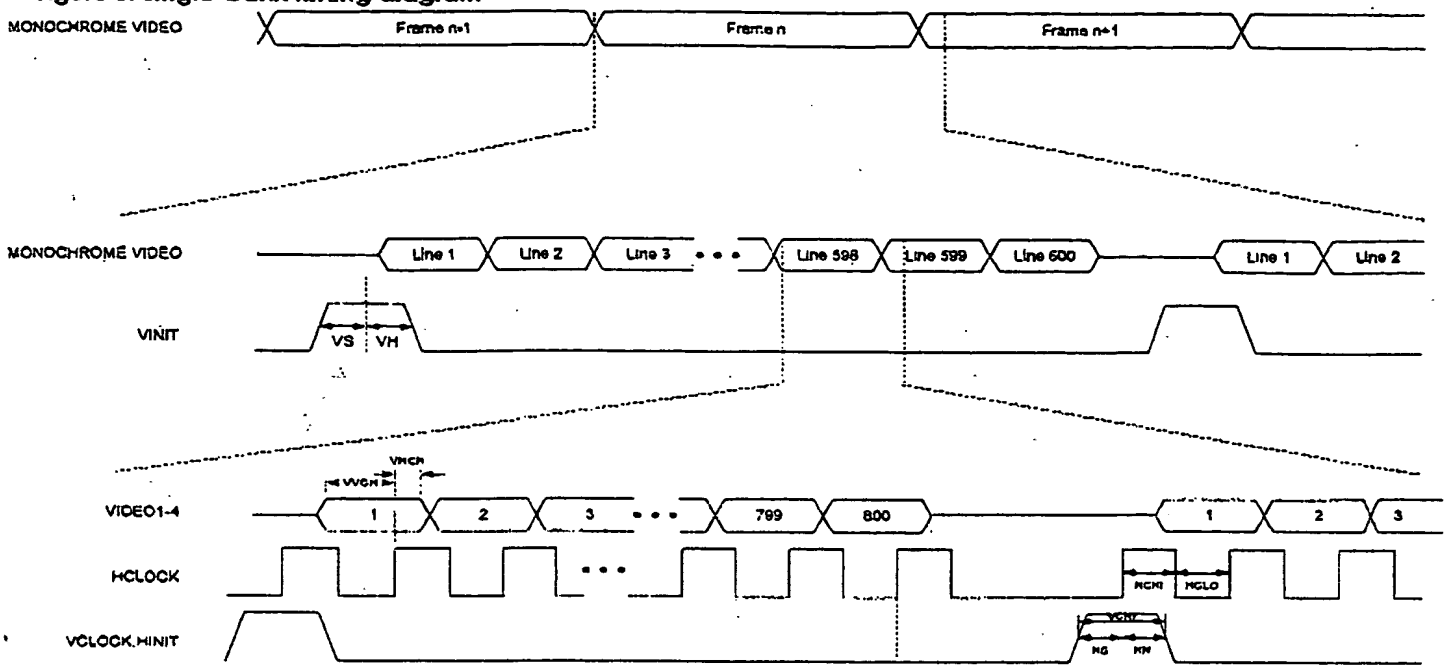


FIG. 6

Architecture

Figure 5 shows a simplified functional diagram of the device in single-bank mode. Each HSR stage controls one column line, and the HSR advances by one pixel column from left to right at every HCLOCK rising edge. Figure 6 illustrates the recommended single-bank timing.

Figure 6: Single-bank timing diagram



Single Bank Mode:
SBSEL = 1, LOADROW = 1, FLASHCLEAR = 0

Horizontal Timing

The timing signals for each line of video consist of the following sequence of events:

1. VCLOCK and HINIT are simultaneously asserted during the very first HCLOCK pulse to advance the vertical shift register and to initialize the horizontal shift register.
2. HCLOCK is repeatedly pulsed to sample the video value.

Vertical Timing

The timing for each frame of video consists of the following sequence of events:

1. VINIT is asserted during the very first VCLOCK to initialize the vertical shift register.
2. VCLOCK is repeatedly pulsed to advance the current line.

Multi-bank Mode (field sequential color)

In this mode, four analog pixel values are delivered to the display during each cycle. By parallelizing the video path, this mode relaxes the speed requirements of individual video channels in both the MD800G6 display and its supporting circuitry. Figure 7 shows a simplified functional diagram of the device in multi-bank mode. Each HSR stage controls four adjacent column lines and the HSR advances by four pixel columns at every HCLOCK rising edge. The multi-bank mode requires only 200 HCLOCK pulses per video line, compared to 800 for the single-bank mode.

The four-way parallelism of MD800G6's video path allows four independent video signals to be loaded simultaneously into four adjacent column wires. This arrangement partitions the display into four interleaved banks, each driven by a different video line (see Figure 7). The banks are interleaved in such a way that VIDEO1 connects to columns 1 (the leftmost column), 5, 9,.; VIDEO2 connects to columns 2, 6, 10,...; VIDEO3 connects to columns 3, 7, 11,...; and VIDEO4 connects to columns 4, 8, 12,....

High-Speed Requirements of Field Sequential Color Operation

The multibank mode exists to support the stringent timing requirements of field-sequential color. Field sequential color (FSC) is a technique for producing color images from a grayscale display. In this mode, each frame interval is divided into three field intervals, one each for red, green, and blue. During the red field, the red image component is displayed on the grayscale device while being illuminated with a red light source. Similar operation occurs during the green and blue fields. The user sees a combined color image if the field rate is faster than the fusion frequency of the human eye. The MD800G6 display is designed to operate at a 180 Hz field rate (60 Hz frame rate) to produce high-quality, non-flickering FSC images.

Because four video signals are loaded in parallel, the multi-bank mode enables faster frame update than single-bank mode. In standard VGA and NTSC, this leaves a larger fraction of the field time for the liquid crystal to settle, resulting in improved contrast, brightness and image fidelity. It is recommended that the multi-bank mode be used in all full-resolution FSC applications.

Figure 7: Functional diagram, multi-bank mode

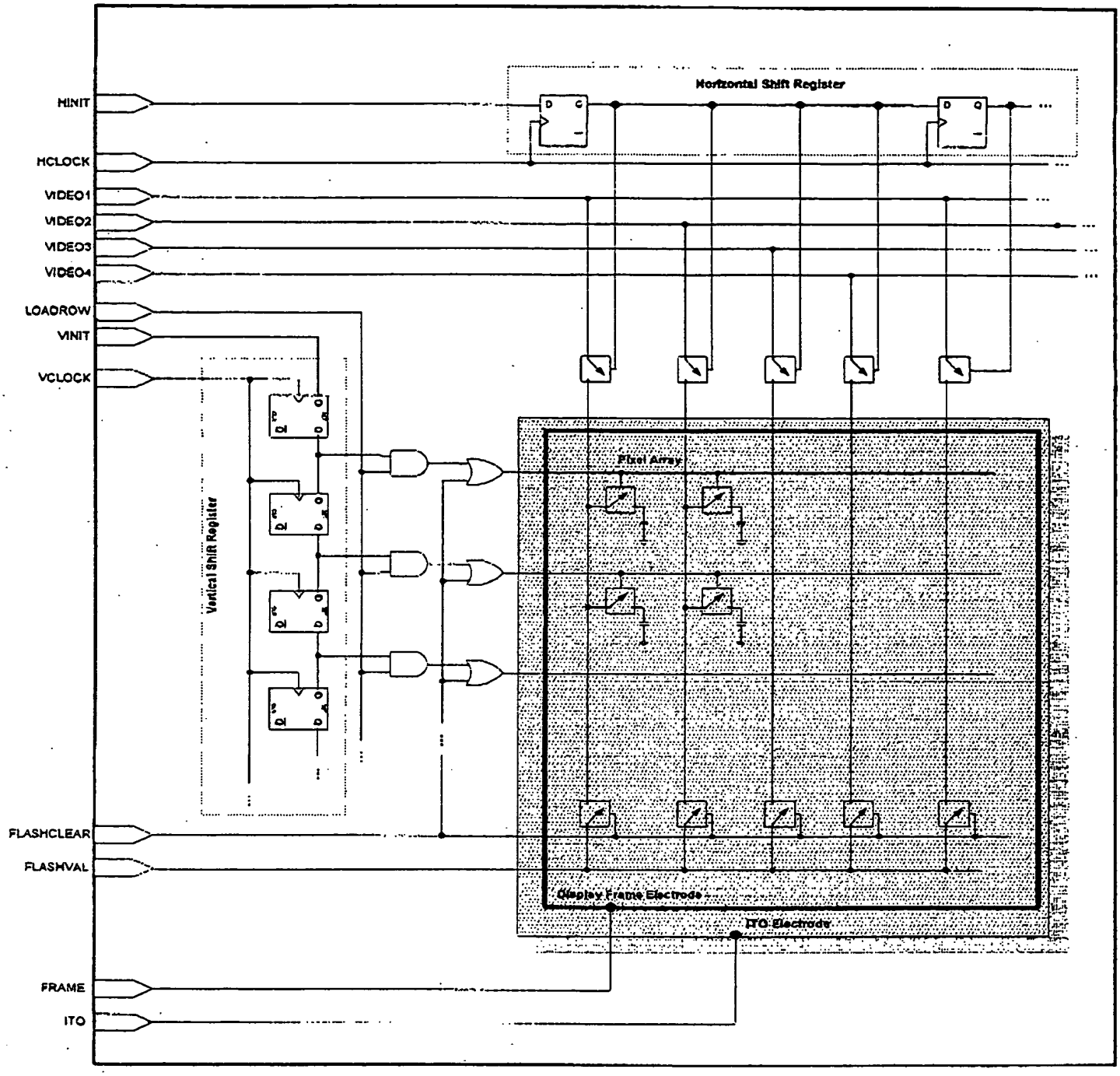
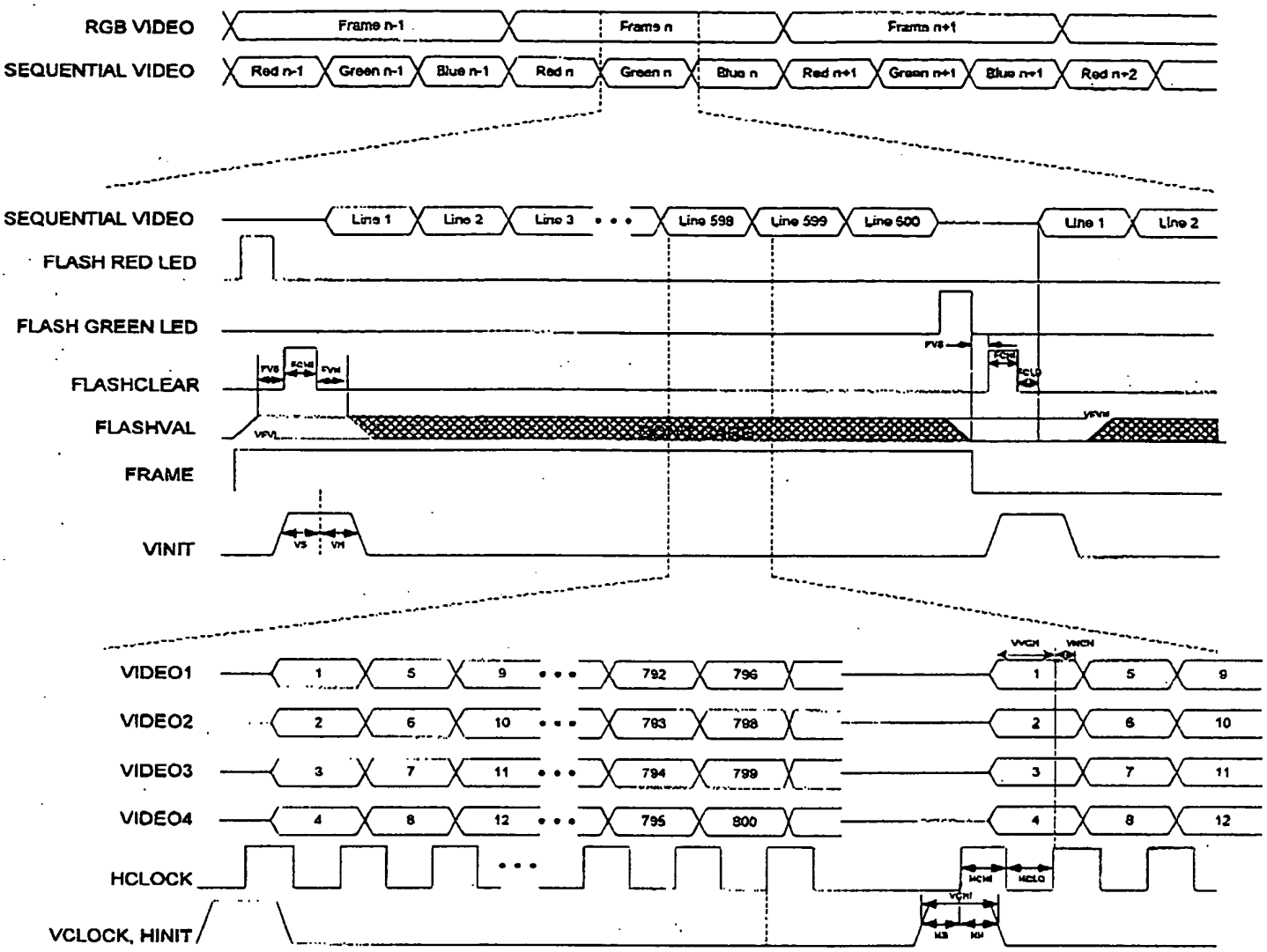


Figure 8: Multi-bank timing diagram



Multi-bank Mode:
SBSEL = 0, LOADROW = 1

Horizontal Timing

The timing signals for each line of video consist of the following sequence of events:

1. VCLOCK and HINIT are simultaneously asserted during the very first HCLOCK pulse to advance the vertical shift register and to initialize the horizontal shift register.
2. HCLOCK is repeatedly pulsed to sample the video value.

Vertical timing

The timing for each of the red, green, and blue fields of video consist of the following sequence of events:

1. FLASHCLEAR is asserted to pre-load the pixel array.
2. FLASHCLEAR is unasserted to resume the regular operation.
3. VINIT is asserted during the very first VCLOCK to initialize the vertical shift register.
4. VCLOCK is repeatedly pulsed to advance the current line.
5. Color light sources, such as red, green, and blue LEDs, are pulsed after their respective fields have been loaded in the pixel array.

Flash-clear function

The flash-clear function loads the voltage presented on FLASHVAL on all the pixels when FLASHCLEAR is asserted. More specifically, when FLASHCLEAR is high, the addressing functions of the shift registers are overridden. All rows of pixels are simultaneously activated, and all the columns are connected to the FLASHVAL input.

The flash-clear function is used to equalize the pixel voltages before video data is scanned, thereby driving the liquid crystal to an optimal initial state from which transitions can be effected at maximum speed. The flash-clear function should always be used when the MD800G6 displays field-sequential color images.

FLASHVAL must be strongly driven to the desired voltage (V_{FVH} or V_{FVL}) to ensure that the highly-capacitive pixel array is appropriately driven during the brief FLASHCLEAR pulse. When the polarity of the video signal with respect to V_{ITO} alternates from field to field, the polarity of FLASHVAL with respect to V_{ITO} should match that of the upcoming video field. For example, at the beginning of a "positive" video field (video signal > 2.5 V), FLASHVAL should be driven to V_{FVL}; at the beginning of a "negative" video field (video signal < 2.5 V, FLASHVAL should be driven to V_{FVL}.

To avoid excessive current dissipation in the video path and/or excessive device stress, the following precautions should be observed:

- No HSR stage should contain a 1. When the typical clocking schemes described above are employed, FLASHCLEAR should only be asserted after the 201st HCLOCK rising edge after the last HINIT pulse in multi-bank mode.

6. RC Timing Models

It is recommended that the high-performance multi-bank mode be employed in all applications with demanding timing requirements. It is further recommended that the output impedance of the source driving the video inputs not exceed 12 Ω. The video-path models below should help the user develop accurate timing estimates. These models apply only to the multi-bank configuration.

Video Input Impedance

The video input is a complex load and should not be treated as a single, lumped capacitance. The circuit model consists of two distributed RC lines linked by a resistive switch. The first RC line has a worst case resistance of 7 ohms and worst case capacitance of 13 pF. The second RC line has 305 ohms and 4.1 pF, respectively.

Figure 9: Video signal path

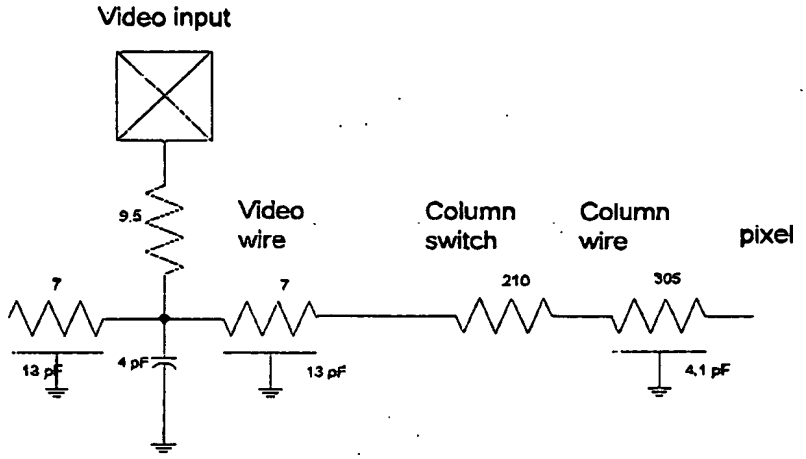
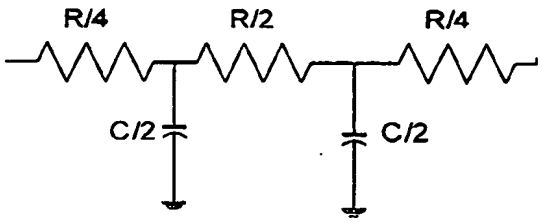


Figure 10: A distributed RC



Each distributed RC line in Figure 9 can be modeled to high accuracy as a lumped load as shown in Figure 10.

7. Display Frame

The MD800G6 display incorporates a 63 µm wide frame around the active display area. The FRAME pin controls the voltage on this frame. The simplest method of configuring the frame is to connect it to the ITO pin, leading to zero applied voltage between the border and ITO, and therefore, a reflective (white) frame. To create a more visually pleasing black frame, the FRAME pin should be switched between the maximum and minimum video voltages at the minimum AC alternation rate. Conveniently, these voltages can be 0 and 5 volts, so that the FRAME pin can be driven by a digital output.

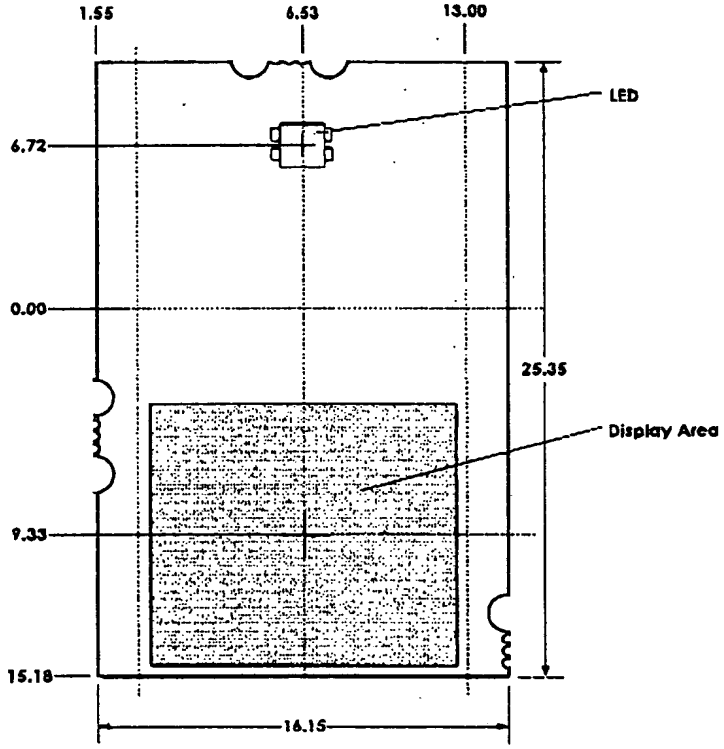
8. Package Options

The MD800G6 display is available on two display carriers.

Eyepiece display carrier

The MD800G6 display is housed on the display carrier pictured below when accompanied by the LookingGlassIII eyepiece. All measurements are in millimeters.

Figure 11: Display Carrier

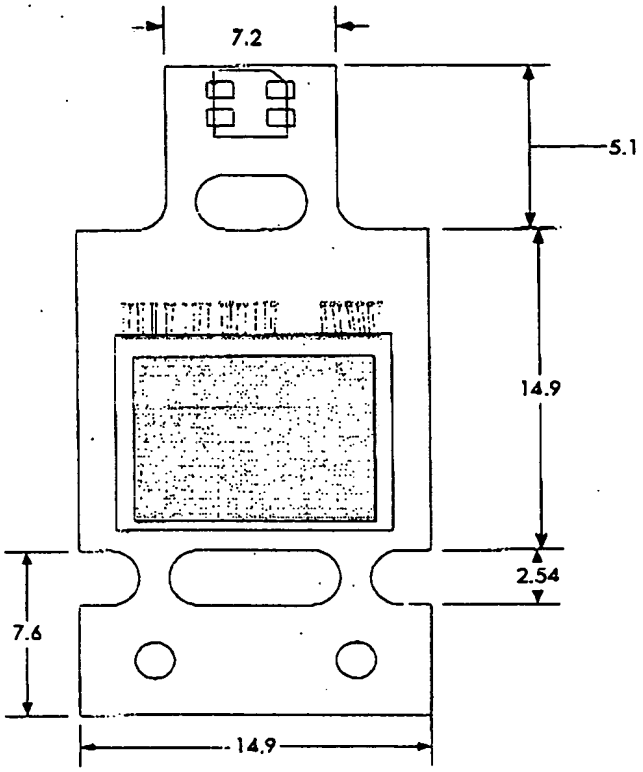


This carrier is hardwired for multi-bank mode with SBSEL tied low internally.

Tabbed Display Carrier

The MD800G6 micromonitor is housed on the display carrier pictured below when it is not shipped with the LookingGlassIII eyepiece.

Figure 12: Tabbed Display Carrier

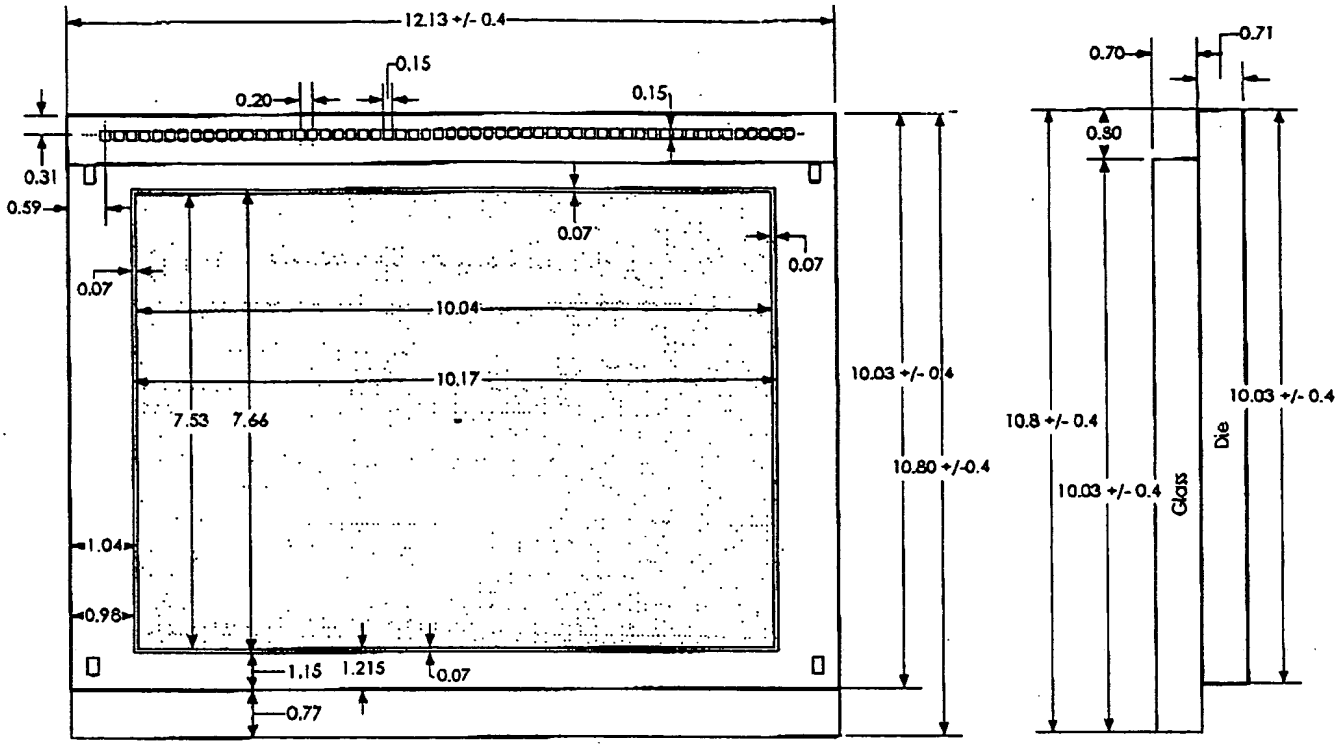


This carrier is hardwired for multi-bank mode. SBSEL is tied low internally.

Display Cell Dimensions

The following diagram shows the dimensions of the bare die of the display. All measurements are in millimeters.

Figure 13: .Bare Die Dimensions



Note: The dimensions given in these drawings are for displays used in Evaluation Kits only. Follow on orders may involve design size changes which will be determined once product specifications are known.

TABLE 8: Display Carrier Pin Numbers

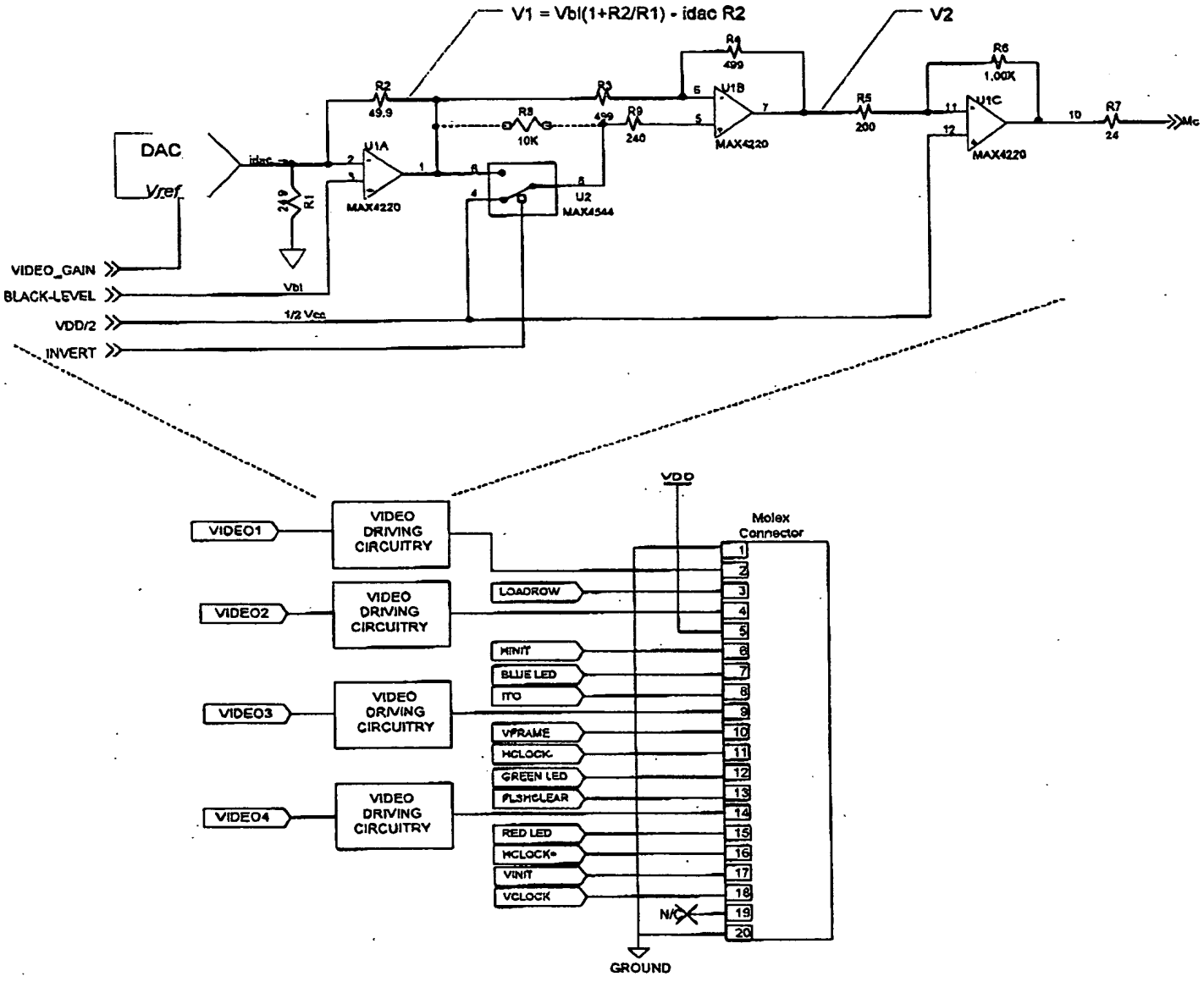
Pin	Name	Description
1	GROUND	Ground pad.
2	VIDEO1	Analog video input - drives columns 1, 5, 9,....
3	LOADROW	Loads video data into addressed pixel row (tie high).
4	VIDEO2	Analog video input - drives columns 2, 6, 10,....
5	V_{DD}	Supply.
6	HINIT	Initialization signal - horizontal shift register.
7	BLULED	Cathode of blue LED - connects to optional field sequential color eyepiece.
8	ITO	Connection to transparent electrode on coverglass.
9	VIDEO3	Analog video input - drives columns 3, 7, 11,....
10	V_{DDLED}	Anode of LEDs - connects to optional field sequential color eyepiece.
11	HCLOCK+	Horizontal shift register clock, LVDS input.
12	GRNLED	Cathode of green LED - connects to optional field sequential color eyepiece.
13	FLASHCLEAR	Connects entire pixel array to FLASHVAL.
14	VIDEO4	Analog video input - drives columns 4, 8, 12,...
15	REDLED	Cathode of red LED - connects to optional field sequential color eyepiece.
16	HCLOCK-	Horizontal shift register clock, LVDS input.
17	VINIT	Initialization signal - vertical shift register.
18	VCLOCK	Vertical shift register cloc.k
19	NC	No connect - reserved.
20	GROUND	Ground.

20-pin Molex connector part #: 52746-2090.

9. Typical Application

This section describes an analog circuit designed to drive the display video input. The circuit allows convenient analog adjustment of contrast and brightness, and performs the AC-preserving inversion function in the analog domain. These functions could also be performed by a digital front end, simplifying the analog path considerably.

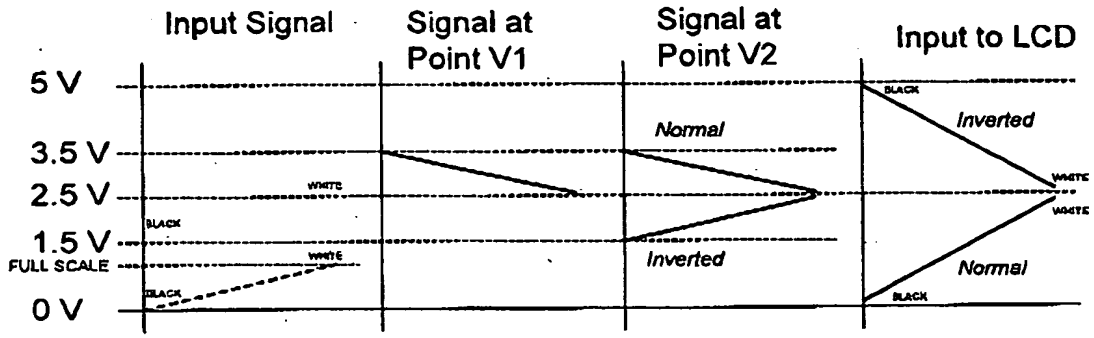
Figure 14: Typical Application



Circuit Description

This circuit uses a Maim MAX4220 Quad Op Amp, and a Maxim MAX4544 Analog switch to condition a signal from a current output DAC into a suitable form for driving the MD800G6. The Video Gain input adjusts the D/A converter for a nominal full scale output current of 10 mA. Zero current yields a black pixel, and full scale current represents a white, or fully reflective pixel. The Black Level input is a low impedance voltage nominally set to 1 V. U1A (1/4 of a MAX4220) converts the DAC current into a 0.5 V pp signal inverted and with a nominal 2.5 V offset from ground. U1B and U2 (MAX4544) invert the sense of the signal about the $V_{dd}/2$ point, or pass it straight through depending on the state of the digital input INVERT. In frame inversion mode INVERT is toggled at the field rate, in line inversion mode INVERT is toggled at the line rate. R8 is an optional resistor which may be installed to prevent the U1B output from driving to the rails during the brief interval while U2 is switching and U2 pin 5 is effectively an open circuit. U1C then performs the final output scale of 5 so the video input of the MD800G6 display sees a 2.5 to ~0.05 V input swing during inverted video, and a 2.5 to ~4.95 V input swing during non-inverted video. R7 is an optional series termination which may be used when driving a long cable.

Figure 15: Circuit Waveforms



Notes:

Optimize Drive Scheme Notes

We have successfully removed the flicker that we had encountered with driving the non-image sticking LC recipe at 60Hz. What remains unknown is whether or not that flicker will be reintroduced over time. When considering whether to drive the display at 60 Hz or 80 Hz, it is important to know that if flicker is reintroduced, it will eventually effect both 60 Hz and 80 Hz driven displays. The displays driven at 80 Hz will just survive a bit longer without evidence of flicker.

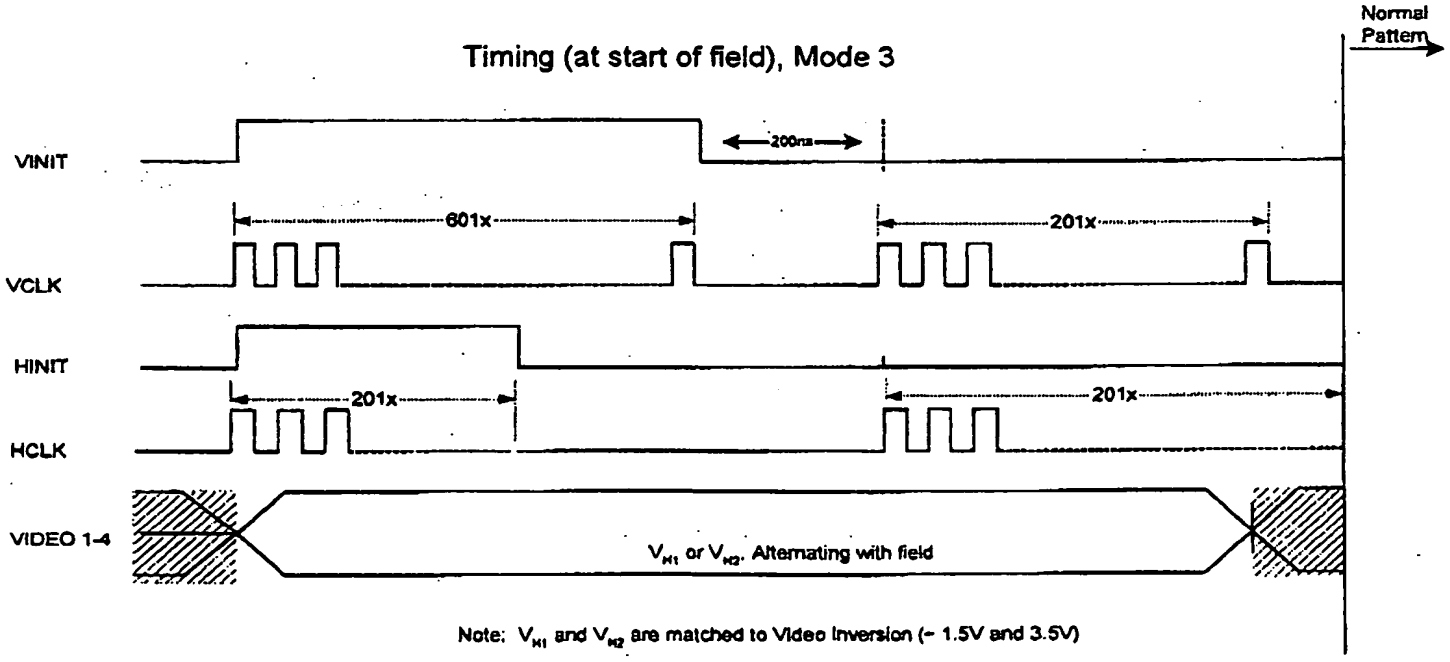
Optimize can choose either drive scheme, but MicroDisplay recommends driving the displays at 60 Hz. This will provide Optimize with superior image quality, and we will solve flicker if it becomes a problem. We want to remain in close contact with Optimize as you test your first shipment of displays so we can head off any problems as you encounter them.

Timing:

At start of frame, the entire display needs to be set to a particular voltage (V_H). This can be done with the dedicated on-chip circuitry or through the video channel.The use of the dedicated "FLASHVAL" analog input requires a DAC at the display, but is the fastest, requiring only 200ns overhead per field.

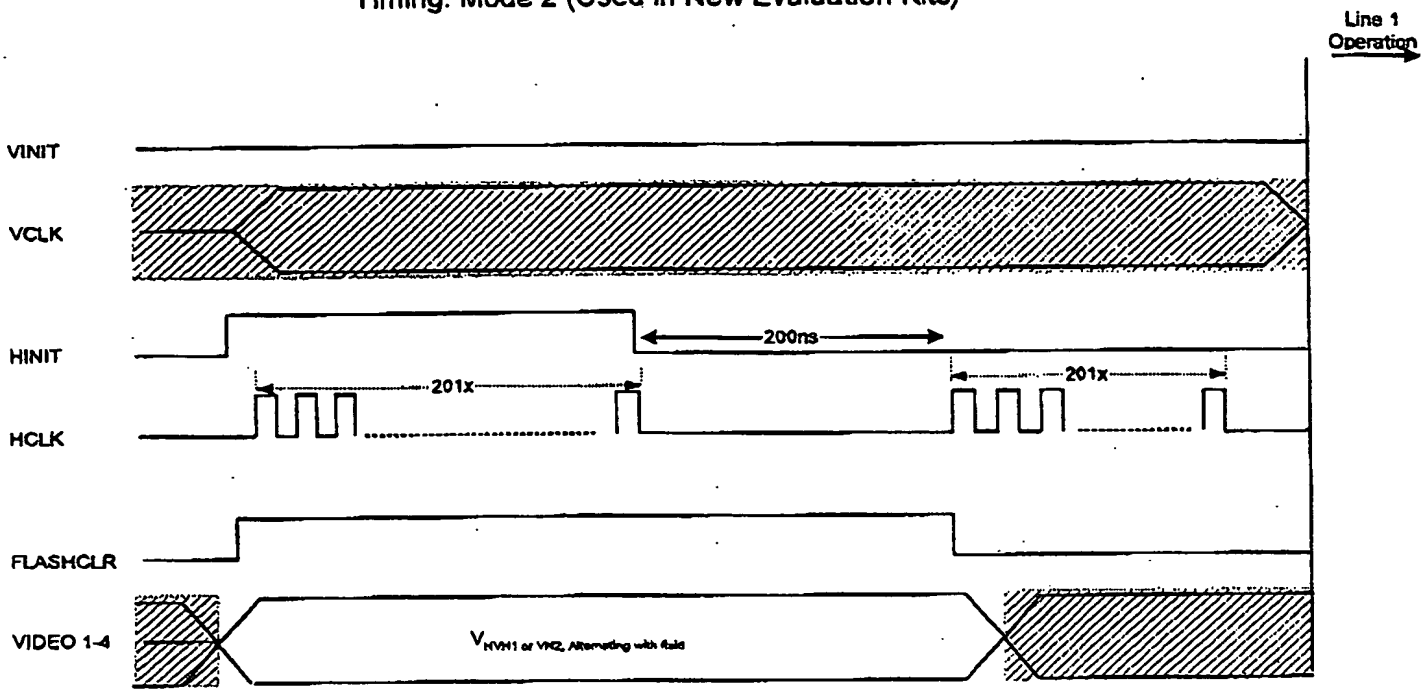
Using "flash clear" to enable all rows in conjunction with providing the V_H value through the video channel requires 2 x200 pixel clocks + 200ns. This mode requires decoding "flash clear" at the head.

The scheme with least on-head circuitry drives all signals through the regular video and timing channels, but requires an additional 2x600 pixel clocks to load up the vertical shift register. This overhead is minimal, and we recommend this scheme. Actually, since the horizontal and vertical registers can be clocked simultaneously, the overhead is 2x600 pixel clocks + 200ns.



Note: V_{H1} and V_{H2} are matched to Video Inversion (~ 1.5V and 3.5V)

Timing: Mode 2 (Used in New Evaluation Kits)



Note: If Optimize has something like FLASHCLEAR decoding (due to CMD compatibility), then mode 2 is better because it has a lower bandwidth.

The remaining major drive issue is fixed vs. changing (flipping) ITO.

While the next lots of 50 and 500 will operate well with the current fixed (2.5V) ITO voltage, the major order for 8000 will probably be passivated and therefore require "flipping" ITO between 0 and 5.

The implications (aside from inverting video voltages appropriately) to drive scheme design is that an ITO flip circuit at the head is required.

If you have any questions about this document, please feel free to contact Stephanie. And let us know what you think about this issue and any others that crop up as you begin receiving displays. Keep in touch with us as you receive and test displays so we can help in any way possible.